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# S.E. (Electronics) (Part - II) (Semester - III) (Revised) Examination, April - 2019

## ENGINEERING MATHEMATICS - III

## Sub. Code : 63434

**Day and Date : Friday, 26 - 04 - 2019** **Total Marks : 100**

**Time : 10.00 a.m. to 01.00 p.m.**

**Instructions :** 1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Use of non programmable calculator is allowed.**

## SECTION - I

***Q1)*** Solve any two. **[18]**

a) Solve : $(D^3 - 3D^2 + 4D - 2)y = e^x + \cos x$

b) Solve : $(D^3 - 7D - 6)y = e^{2x}(x + 1)$

c) Solve : $(D^2 + 2D + 1)y = x \cos x$

d) The differential equation of a circuit is $R\frac{dq}{dt} + \frac{q}{c} = 40\,e^{-3t} + 20\,e^{-6t}$.

If R = 20 ohms, C = 0.01 farad and q = 0 at t = 0, show that the minimum charge on the capacitor is 0.25 coulombs.

***Q2)*** Solve any two. **[16]**

a) i) Find the angle between the normals to the surface $xy = z^2$ at the points (1, 4, 2) and (–3, –3, 3)

ii) Find the directional derivative of $\phi = x^2y \cos z$ at $(1, 2, \pi/2)$ in the direction of $\bar{a} = 2i + 3j + 2k$.

b) A vector field is given by $\bar{F} = (x^2 + xy^2)i + (y^2 + x^2y)j$. Show that $\bar{F}$ is irrotational and find its scalar potential. Also find Grad (Div $\bar{F}$).

c) Compute the divergence and curl of vector

$$\bar{F} = \frac{x}{r}i + \frac{y}{r}j + \frac{z}{r}k \text{ where } r = \sqrt{x^2 + y^2 + z^2}$$

***P.T.O.***

*Q3)* Solve any two. **[16]**

a) If mean and variance of a Binomial distribution are 4 and 2 respectively, find the probability of

i) exactly 2 successes

ii) less than 2 successes

iii) atleast 2 successes

b) A firm produces articles of which 0.1 percent are defective. It packs them in cases each containing 500 articles. If a wholesaler purchases 100 such cases how many cases can be free from defectives, how many can be expected to have one defective.

c) In a sample of 100 dry cells tested to find the length of life produced the following results : Mean = 12 hours, standard deviation = 3 hours.

Assuming the data to be normally distributed, what percentage of battery cells are expected to have life

i) More than 15 hours?

ii) Less than 6 hours?

iii) Between 10 and 14 hours?

[Given : For S.N.V. z area between $z = 0$ to $z = 1$ is 0.3413, area between $z = 0$ to $z = 2$ is 0.4772, area between $z = 0$ to $z = 0.67$ is 0.2485]

## SECTION - II

*Q4)* Attempt any three from the following :

a) Find Laplace transform of $(1 + 2t - 3t^2 + 4t^3)\, H(t - 2)$. **[6]**

b) Find inverse Laplace transform of

$$\frac{S^2 - 3}{(S+2)(S-3)(S^2+2S+5)}.$$ **[6]**

c) Solve using Laplace transform

$(D^2 + 4D + 8)\, y = 1$, with $y = 0$, $Dy = 1$ at $t = 0$. **[6]**

d) Evaluate using Laplace transform

$$\int_0^\infty \frac{\cos 6t - \cos 4t}{t}\, dt.$$ **[6]**

*Q5)* Attempt any two of the following :

a) Express $e^{-x}$ in a fourier series over $-\pi \le x \le \pi$. [8]

b) Find a fourier series with period 3 to represent $f(x) = 2x - x^2$ in the range [0, 3]. [8]

c) Find a series of cosines of multiples of $x$ which will represent $x \sin x$ in the internal $[0, \pi]$ and show that $1+\frac{2}{1.3}-\frac{2}{3.5}+\frac{2}{5.7}\ldots\ldots\infty = \pi/2$. [8]

*Q6)* Attempt any two of the following :

a) Using fourier integral, show that

$$\int_0^\infty \frac{1-\cos\pi\lambda}{\lambda}\sin x\lambda\, d\lambda \quad \begin{matrix} = \pi/2, & 0 < x < \pi \\ = 0, & x > \pi \end{matrix} .$$ [8]

b) Find the fourier transform of the function

$$f(x) = 1+\frac{x}{a}, \quad (-a < x < 0)$$
$$= 1-\frac{x}{a}, \quad (0 < x < a)$$
$$= 0, \quad \textit{otherwise}$$ [8]

c) Find fourier sine and cosine transform of

i) $x^{n-1}$,

ii) $\frac{1}{\sqrt{x}}$.

[8]

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# S.E. (Electronics) (Semester - III) Examination, May - 2019
# ELECTRONIC MEASUREMENT AND INSTRUMENTATION
## Sub. Code : 63435

**Day and Date : Thursday, 02 - 05 - 2019** **Total Marks : 100**

**Time : 10.00 a.m. to 01.00 p.m.**

**Instructions :** 1) **All questions are compulsory.**

2) **Figures to the right indicate full marks.**

## SECTION - I

*Q1)* Attempt any two of the following : **[16]**

a) Elaborate the working of Dual trace Oscilloscope.

b) Explain in detail the different factors affecting on the selection of Instrument for measurement.

c) Draw block diagram of measuring system and explain each block in detail.

*Q2)* Attempt any two of the following : **[16]**

a) Explain the operation of digital measurements of mains frequency.

b) Explain the operating principle of a ramp type DVM.

c) Draw a neat and labeled diagram of Cathode ray tube and explain its working.

*Q3)* Write short note on any three of the following : **[18]**

a) CRO probes

b) Digital frequency meter

c) Calibration of Instrument

d) Pulse generator

*P.T.O.*

## SECTION - II

*Q4)* Attempt Any Two : **[16]**

a) What is basic principle of Strain Gauge? Explain construction of Strain Gauge.

b) Derive Bridge Balance condition for Hays Bridge. State advantages.

c) Draw the block diagram and explain single slope A/D Converter.

*Q5)* Attempt Any Two : **[16]**

a) What is piezoelectric effect? Explain the working of piezoelectric transducer.

b) What are objectives of DAS ?Explain multichannel DAS with neat block diagram.

c) Explain Andorsens Bridge.

*Q6)* Write short notes on (Any three) : **[18]**

a) Wheatstones Bridge

b) Cold junction compensation

c) Sample and hold circuit

d) Selection criterion of Transducer

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# S.E. (Electronics Engg.) (Semester - III) (Revised)
## Examination, May - 2019
## ELECTRONICS CIRCUIT ANALYSIS AND DESIGN - I
## Sub. Code : 63436

**Day and Date : Saturday, 04 - 05 - 2019** **Total Marks : 100**

**Time : 10.00 a.m. to 01.00 p.m.**

**Instructions :**
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Standard Data sheet is allowed.**

## SECTION - I

***Q1)*** Attempt any two of the following. **[8 marks each]**

a) Explain construction, working, advantages, dis-advantages of center tapped full wave rectifier with suitable circuit diagram & waveforms.

b) Bridge type full wave rectifier circuit is supplied from a 10V, 50Hz supply with step up ratio of 1:2 to a resistive load of 8.2KΩ. The diode forward resistance is 50Ω & transformer secondary resistance is 15Ω Determine
   i) Average/mean/ DC voltage,
   ii) RMS/ripple current through load,
   iii) Rectification efficiency,
   iv) Maximum power delivered to load.

c) Design an unregulated power supply with inductor filter to produce 12V, 25mA with ripple factor of 4%.

***Q2)*** Attempt any two of the following. **[8 marks each]**

a) Design Zener shunt regulator to produce Vo = 6V from an input of 15V unregulated power supply.

b) Explain the following
   i) Line & load regulation
   ii) Short circuit & overload protection circuit

c) Design transistorized shunt regulator to produce $V_o$ =5V, $I_o$=100mA, Vin : 10 to 25V.

***P.T.O.***

*Q3)* Attempt any three of the following. **[6 marks each]**

a) Explain the double level clipping Circuits (Slicer & Limiter). Draw its waveforms & transfer curve.

b) What is Pulse input? Explain the response of high pass filter circuit to pulse input for RC<<T & RC ≥ T with waveform of voltage across capacitor & output.

c) The voltage doubler circuit produce 2 % maximum output ripple across the load resistor of 27 KΩ for the input of ± 12 V, 10 KHz Square wave. Determine the values of capacitors Cl and C2.

d) Determine the output voltage ($V_o$) also sketch input & output waveforms for the clamper circuits with the given data: Positive Clamper for which Vi =18V p-p (square wave), with ideal & practical diode.

## SECTION - II

*Q4)* Attempt any three of the following. **[6 marks each]**

a) Write short note on bias compensation techniques.

b) Draw h-parameter model for common Base amplifier and write equations for all h- parameters.

c) Compare BJT and JFET.

d) Design self bias circuit with $h_{FE}$ =100, $V_{cc}$ = 12V, $V_{CEQ}$=5V, $I_{CQ}$ = 4mA.

*Q5)* Attempt any two of the following : **[8 marks each]**

a) A transistor circuit using voltage divider biasing circuit has the following components. $R_C$= 2.2KΩ, $R_E$=3.3KΩ, $R_1$=6.8KΩ, $R_2$=4.7KΩ. The supply voltage $V_{CC}$=15V. Analyze the circuit to determine $V_{CE}$ & $I_C$. Also calculate stability factor. Consider β =100.

b) Design single stage RC coupled amplifier with following specifications. Av =100, S=11, Vopp=4V, $V_{CC}$=12V, hfe-100, fin =100Hz to 1MHz.

c) Draw approximate short circuit high frequency model. Derive expression for unity gain bandwidth product ($f_T$) in terms of gm and $C_{b,e}$.

*Q6)* Attempt any two of the following. **[8 marks each]**

a) Draw and explain in detail low and high frequency step response of RC coupled amplifier in terms of rise time & % sag.

b) Draw a neat diagram of common source FET amplifier. Derive an expression for its voltage gain at low frequency.

c) A transistor is used in CE amplifier at quiescent collector current of 0.1mA. If the load resistance is 5.6 KΩ and RS=600Ω. Calculate: Ai, Ri, Av, Ro having h-parameters $h_{ie}$ = 6.4KΩ, $h_{re}$ = 1.5 × $10^{-4}$ , $h_{fe}$= 240, $h_{oe}$= 6μ mho.

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# S.E. (Electronics) (Semester - III) Examination, May - 2019

## ANALOG COMMUNICATION

## Sub. Code : 63437

**Day and Date : Tuesday, 07 - 05 - 2019** **Total Marks : 100**

**Time : 10.00 a.m. to 01.00 p.m.**

**Instructions : 1) All questions are compulsory.**

**2) Figures to the right indicates full marks..**

## SECTION - I

*Q1)* Solve any three. **[18]**

a) Derive an expression of an amplitude modulated wave voltage which contains three terms unmodulated carrier, LSB and USB.

b) Comment on types of distortion arises in diode detector.

c) Draw and explain reactance modular used in FM generation.

d) Explain

i) Baseband signal

ii) Carrier signal

iii) Modulated signal

e) In a PM system, when the audio frequency (AF) is 500 HZ, and the AF voltage is 2.4 V, the deviation is 4.8 kHz. If the AF voltage is now increased to 7.2 V, what is the new deviation? Find the modulation index in each case.

*Q2)* Solve any two. **[16]**

a) A Sinusoidal carrier signal of 5 V peak amplitude and 100 kHz frequency is amplitude modulated by a 5 kHz signal of peak amplitude of 3 V. What is the modulation index? Draw the two sided spectrum of modulated signal.

b) Draw and explain pre-emphasis and De-emphasis circuit with emphasis curve.

c) Define AGC. Explain different types of AGC, also explain how AGC principle is used in radio receiver.

*P.T.O.*

*Q3)* Solve any two. **[16]**

a) Why modulation is necessary? Explain various types of modulation?

b) Draw block diagram of tuner used in AM Radio receiver with waveforms and explain in detail.

c) Derive an expression of a frequency modulated wave voltage.

$v_{FM} = V_c Sin\ (w_c t + m_f cosw_m t)$

## SECTION - II

*Q4)* Solve any three. **[18]**

a) Draw and explain FM receiver block diagram and comment on basic differences to that of AM receiver.

b) Explain the following terms in detail.

i) Natural sampling

ii) Flat top sampling

c) Define noise. Comment on various types of noise.

d) Draw PWM modulator circuit and explain.

e) Explain antenna term Radiation pattern in detail with diagram.

*Q5)* Solve any two. **[16]**

a) Explain PLL is used for frequency Demodulation.

b) What are various types of PTM? Explain with waveforms generation of PTM signals using indirect method.

c) What is ground wave propagation? Explain.

*Q6)* Solve any two. **[16]**

a) Draw and explain Travis detector in FM Demodulation with characteristics.

b) What is time division multiplexing? Explain in details with the help of diagram.

c) Explain in brief

i) Folded dipole antenna

ii) Yagi-Uda antenna

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# S.E (Electronics) (Semester - III) Examination, May - 2019
## NETWORK ANALYSIS
## Sub. Code : 63438

**Day and Date :Thursday, 09 - 05 - 2019** **Total Marks : 100**

**Time : 10.00 a.m. to 01.00 p.m.**

**Instructions:**
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**

## SECTION - I

*Q1)* Attempt any two. **[16]**

a) Draw the oriented graph of the circuit given in Figure 1. Draw the various possible Trees and Co Trees for the given circuit.

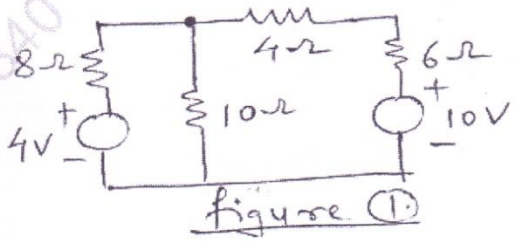


figure ①

b) Find the current flowing through the 10 Ω resistance using Mesh Current Analysis technique in Figure 1.

c) Derive equations for star to Delta Transformation and Delta to star Transformation in case of resistive circuit.

*Q2)* Attempt any two. **[16]**

a) Find the current flowing through 10 Ω resistance by the application of Norton's Theorem in Figure 2.

b) Find the current flowing through the 10 Ω resistance for the given circuit in figure 2 using superposition theorem.

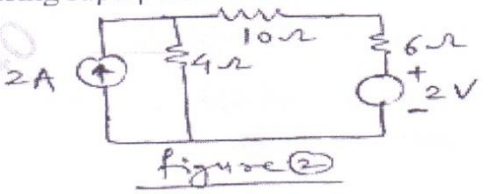


figure ②

*P.T.O.*

c) Derive the condition for maximum power Transfer in a resistive circuit.

*Q3)* Write short notes on any three: **[18]**

a) Find the equivalent parameters in case of two, port networks connected in parallel

b) Derive the Y parameters in terms of hybrid h parameters.

c) Derive the Z parameters of a symmetrical T network.

d) Find the ABCD parameters for the circuit given in figure 3.

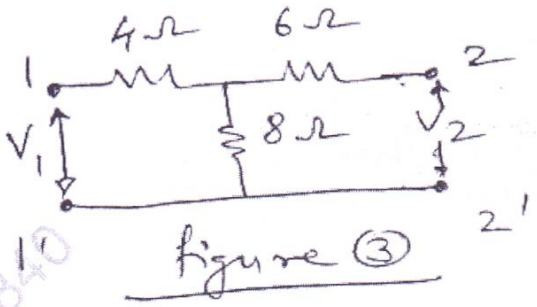



figure ③

## SECTION - II

*Q4)* Solve any two: **[2×8=16]**

a) Explain in brief the concept of poles and zeros of network functions. Mention the restrictions on poles and zeros for transfer functions.

b) A low pass filter composed of symmetrical π section. Its series arm includes 0.02 H inductance and each shunt arm includes 2μF capacitor. Find:

i) Cut oof frequency

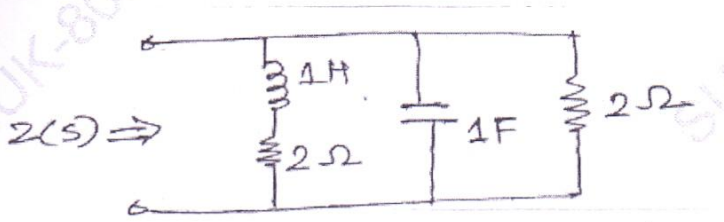
ii) Characteristic impedance at 200 Hz & 2000Hz

iii) Characteristic impedance at zero frequency.

c) Derive the relationship between bandwidth, resonance frequency and quality factor for series resonance circuit.

*Q5)* Solve any two: **[2×8=16]**

a) Find driving point impedance for network shown in fig.




b) Design symmetrical bridged T attenuator with attenuation of 20 dB and terminated into load of 500Ω.

c) Write note on composite filter.

*Q6)* Solve any three: **[3×6=18]**

a) Derive equation for resonance frequency of parallel resonance circuit.

b) Design constant - K high pass filter (T & π section) with cutoff frequency 2.1 KHz. and design impedanace of 400Ω.

c) Expalain in detail inverse networks.

d) Design symmetrical T-pad attenuator to give attenuation of 60 dB and to work in line of 500Ω impedance.

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# S.E. (Electronics) (Semester - IV) (Revised) Examination, May - 2019

## LINEAR INTEGRATED CIRCUITS

## Sub. Code : 63440

**Day and Date : Tuesday, 14 - 05 - 2019** **Total Marks : 100**

**Time : 02.30 p.m. to 05.30 p.m.**

**Instructions :** 1) **All questions are compulsory.**
2) **Assume suitable data if necessary.**
3) **Figures to right indicate full marks.**

*Q1)* Solve any two of the following : **[18]**

a) Explain the working of transistorized differential amplifier. What is need of dual power supply?

b) Explain with neat circuit diagram constant current bias.

c) Explain the different parameters in transistorized differential amplifier.

*Q2)* Solve any two of the following : **[16]**

a) Explain with neat diagram frequency Vs gain characteristics of Opamp. and explain the following parameters

i) Frequency response

ii) Gain bandwidth product

iii) Gain rolloff

b) Explain different methods of compensation techniques

i) Input output offset voltage

ii) Input output offset current. Draw necessary circuit diagram.

c) An opamp has unity gain bandwidth of 1.5 MHz for a signal frequency 2KHz. What is the open loop DC voltage gain?

*P.T.O.*

*Q3)* Solve any two of the following : **[16]**

a) Explain the limitations of openloop configuration. Describe close loop inverting amplifier. Derive the equation of closed loop voltage gain Av.

b) Explain the concept of virtual ground. Derive the gain equations of inverting and non inverting amplifier.

c) For non inverting amplifier Ri = 1KΩ, Rf = 10 KΩ, Determine closed loop voltage gain, feedback factor β & input impedance zi.

*Q4)* Solve any two of the following : **[18]**

a) With neat circuit diagram explain V to I converter with floating load. Derive the equation for output current w.r.t. input voltage.

b) Explain with neat diagram summing amplifier. Derive the equation for output voltage with no.of inputs. How this can be used as average amplifier?

c) Design differentiator using op amp with input signal frequency $f_{max}$ = 200Hz. Also draw the output waveform for square input of lv peak at 200Hz.

*Q5)* Solve any two of the following : **[16]**

a) Derive the equation of transfer function of first order Butterworth lowpass filter. Draw the frequency vs gain response of filter.

b) Design a first order lowpass filter at a cutoff frequency of 2KHz with passband gain of 2. Draw the filter response.

c) Explain with neat diagram first order bandpass filter. Derive the equation of transfer function, Draw its frequency response.

*Q6)* Solve any two of the following : **[16]**

a) Explain with neat diagram working of RC phaseshift oscillator using opamp. Express the equation of frequency of oscillations and required gain at this frequency.

b) With neat internal diagram explain working of IC 555 timer. Express ton & toff period equations.

c) Determine output frequency $f_o$, lock range $\Delta f_l$ & capture range $\Delta f_c$ of PLL 565. Assume R1 = 15KΩ. C1 = 0.01μf, C = 1μf & supply voltage is +12v.

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# S.E. (Electronics Engineering) (Part - II) (Semester - IV) (Revised) Examination, May - 2019

## ELECTRONICS CIRCUIT ANALYSIS AND DESIGN - II

## Sub. Code : 63441

**Day and Date : Thursday, 16 - 05 - 2019** **Total Marks : 100**

**Time : 02.30 p.m. to 05.30 p.m.**

**Instructions :**
1) **All questions are compulsory.**
2) **Figures to right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Standard data sheet is allowed.**

## SECTION - I

***Q1)*** Attempt any three of the following : **[18]**

a) i) An amplifier has an open loop gain of 500 and a feedback factor of 0.05. If the open loop gain changes by 15% due to temperature, find the percentage change in closed loop gain

ii) An amplifier has gain of 300. When negative feedback is applied the gain is reduced to 240. Find the value of feedback factor.

b) A push pull class B audio frequency power amplifier supplies 0.5 W power to 8Ω loudspeaker through an ideal output transformer having center tapped primary winding. Each of the two identical transistor in the circuit has VCE = 0.5V and VCC = 9V Determine:

i) Turns ratio of a transformer.

ii) Power dissipation of each transistor.

c) With the help of neat circuit, explain the operation of push pull class B Power amplifier. Derive an expression for its conversion efficiency.

d) Draw a neat circuit diagram of bootstrapped emitter follower. Derive an expression for Current gain, Input resistance and Voltage gain.

***P.T.O***

**Q2)** Attempt any two of the following : **[16]**

a) Design a direct coupled amplifier which uses identical transistors with the following specifications as : hfemin=100, $I_{CMAX}$=100mA, $V_{CE(max)}$ = 45V. The Circuit parameters are $V_{CC}$=10V, $V_{OPP}$=5V, $R_L$ = 4.7KΩ, $AI_{CQ}$ allowed is 2.5%, fo = 50H and stability factor (S) = 10. Calculate individual and overall gain.

b) Design transformer coupled class A power amplifier to deliver as power 2W to a load resistance of 4Ω. The transformer efficiency (η) is 70%. Use VCC =12V. Use transistor data: PDmax = 11W, VCE=45V, ICMAX=3A, hfemin = 40.

c) Draw a neat schematics of voltage series feedback. Derive an expression for input impedance (Rif), Output impedance (Rof) and Voltage gain (Avf) in terms of feedback Factor (β) and Av'.

**Q3)** Attempt any two of the following. **[16]**

a) Design a two stage common emitter amplifier to meet the following specifications:

i) Load resistance (RL) = 2.2KΩ

ii) Source Resistance (Rs) = 470Ω

iii) Supply Voltage (Vcc) =15V

iv) Peak to peak output Voltage (Vopp) = 6V

v) Lower 3dB frequency (F) = 20 Hz – 20 KHz.

Use Transistor data: PD(max) = 500mW, VCE = 45V, IC(max) = 100mA hfe(min) 20.

b) i) Give the comparison between the different types of power amplifier based on Conducti angle, Position of Q point, Efficiency.

ii) Draw and explain RC Coupled Amplifier with frequency response.

c) Design a bootstrapped emitter follower circuit to provide the following specifications:

Input impedance (Ri) = 470 KΩ, Lower 3dB frequency = 50 Hz, Vo= 3Vpp, Load resistance $R_L$ = 4.7KΩ, Source Resistance (Rs.) = 620Ω.

## SECTION - II

*Q4)* Attempt any three of the following. **[18]**

a) Draw a neat circuit diagram of Phase shift oscillator.
Prove that minimum gain required for sustained oscillation is given by, $h_{fe} \geq 29\ (R/Rc) + 23 + 4\ (Rc/R)$.

b) Explain the operation of step down switch mode power supply with Suitable waveforms.

c) Design an Astable multivibrator for frequency of 1 KHz to give output voltage of 5 V. Use transistor BC 547 with: PD (MAX) =500mW, V CE = 45V, I C (MAX) = 100mA, hfe(Min)= 110.

d) Briefly Explain the Barkhausens criteria and amplitude stability in oscillator.

*Q5)* Attempt any two of the following. **[16]**

a) The fixed bias bistable multivibrator uses following parameters:
Vcc = 12V, –VBB = –8V, R1=10KΩ, R2= 50KΩ, RC= 2.2KΩ, and hfe = 30. Calculate stable state
currents and voltages for VCE (Sat) =0.2V and V BE (Sat) =0.7V.

b) Design a transistorized Colpitts Oscillator for the following specification:
Output Voltage Vo = 3Vrms, Frequency (f) = 1MHz, Av=25
Use transistor BC 147 with PDmax= 250mW, VCE=45V, ICmax = 200mA, hfe= 330, hie= 4.5KΩ.

c) Design an RC phase shift Oscillator using BJT for the following specification:
Peak to Peak Output amplitude = 5V, Frequency of Oscillation (f) = 2 KHz, Use Vec = 12V.

*Q6)* Attempt any two of the following. **[16]**

a) With a neat circuit diagram, explain the working of Hartley oscillator. Derive an expression for frequency of oscillation (f) and minimum gain required for sustained oscillation.

b) i) Write short note on Switching Regulator IC "LM 3524".
ii) Write a short note on: Crystal Oscillator

c) Design a monostable multivibrator for the following specification:
Frequency F = 5 KHz, $V_{CC}$ = 10V, $-V_{BB}$= –5V, $V_{CE(Sat)}$ =0.3V, $V_{BE(SAT)}$=0.6V,
Design of Trigger circuit is expected.

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# S.E. (Electronics Engg.) (Semester-IV) Examination, May - 2019

## DATA STRUCTURES & ALGORITHMS

## Sub. Code : 63442

**Day and Date : Monday, 20 - 05 - 2019** **Total Marks : 100**

**Time : 02.30 p.m. to 05.30 p.m.**

**Instructions :** 1) **Assume suitable data wherever necessary.**
2) **Figures to the right indicate full marks.**

## SECTION - I

*Q1)* Answer **Any Three** of the following. **[18]**

a) Describe the classification of data structure.

b) Write an algorithm for linear search.

c) What is memory allocation & garbage collection?

d) What is two way list? Explain it with suitable diagram.

e) Explain Stack as an abstract data type.

*Q2)* Answer **Any Two** of the following. **[16]**

a) What is meant by records? How records are represented in memory?

b) Write algorithm for insertion of a node at the beginning of a linked list.

c) Write algorithm to evaluate expression written in postfix form.

*Q3)* Answer **Any Two** of the following. **[16]**

a) What is recursion? Explain briefly its properties.

b) What is queue? Explain circular queue with suitable diagram.

c) What is header linked list? Explain its types with suitable diagram.

*P.T.O*

## SECTION - II

*Q4)* Answer **Any Two** of the following. **[16]**

a) Explain the algorithm for Post order traversal of binary tree with example.

b) Explain representation of Binary tree in memory.

c) Explain BFS algorithm with example.

*Q5)* Answer **Any Two** of the following. **[16]**

a) What is collision resolution ? Explain the technique for collision resolution.

b) Explain shortest path algorithm with example.

c) What is hashing? Explain different hash functions.

*Q6)* Write short note on **any three**. **[18]**

a) AVL tree

b) Binary search Tree

c) Depth first search technique

d) Warshall's algorithm

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Total No. of Pages : 2

# S.E. (Electronics Engineering) (Part - II) (Semester - IV) Examination, May - 2019

## DIGITAL SYSTEMS AND MICROPROCESSOR (Revised)

### Sub. Code : 63443

**Day and Date : Wednesday, 22 - 05 - 2019** **Total Marks : 100**

**Time : 02.30 p.m. to 05.30 p.m.**

**Instructions :** 1) **Figures to the right indicates full marks.**
2) **Assume suitable data whenever necessary.**

## SECTION - I

*Q1)* Attempt any three questions **[18]**

a) Reduce the function f(A ,B,C,D) = Σm(0,12.3.8.9,13,15) + d(7,10,11) using K-map and implement using NAND gates.

b) Convert an S-R Flip flop to a D flip flop.

c) What is a hazard? What are different types of hazards?

d) Draw and explain 4-bit Ring counter.

*Q2)* Attempt any two questions **[16]**

a) Design a 4-bit gray to binary code converter.

b) Define mux and implement the following function using 8:1 mux.

F(A,B,C,D,) = Σm(1,2,4,5,9.1 1,13)

c) Explain Carry look ahead adder with neat diagram and relevant expressions. And also briefly explain how it is better than parallel adder.

*Q3)* Attempt any two questions **[16]**

a) Explain Universal Shift Register with the help of logic diagram.

b) Explain RAM, ROM and EPROM.

c) Design an asynchronous mod 5 counter.

*P.T.O.*

## SECTION - II

***Q4)*** Answer any Two of the following. **[2 × 8 = 16]**

a) Draw and Explain de multiplexing of Address and Data bus in 8085.

b) Explain addressing modes of 8085 with example.

c) Draw and Explain Pin out diagram of 8085.

***Q5)*** Answer any Two of the following. **[2 × 8 = 16]**

a) Draw and Explain Machine Cycle of instruction LDA 2000H.

b) Explain functions of following pins of 8085

a. ALE b. ADO-AD7 c. HOLD and HLDA d. Reset in

c) Explain concept of stack in 8085 and stack related instructions in 8085 with example.

***Q6)*** Write short notes on any three of the following. **[3 × 6 = 18]**

a) Timing diagram of instruction ADD B

b) Model of 8255

c) Interrupt structure of 8085

d) Thumb wheel switches

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Total No. of Pages : 3

# S.E. (Electronics Engineering) (Semester - IV) Examination, May - 2019

## CONTROL SYSTEM ENGINEERING

### Sub. Code : 63444

**Day and Date : Friday, 24 - 05 - 2019** **Total Marks : 100**

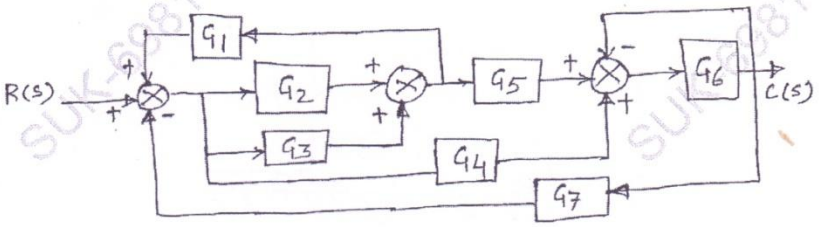
**Time : 02.30 p.m. to 05.30 p.m.**

**Instructions : 1) All questions are Compulsory.**
**2) Figures to the right indicate full marks.**
**3) Assume suitable data wherever necessary.**
**4) Use of graph papers are allowed.**
**5) Use of scientific calculator is allowed.**

## SECTION - I

***Q1)*** Attempt any two **[2 × 9 = 18]**

a) Find C(s)/R(s) for the system shown in fig below using block diagram reduction technique.




b) What is Masons gain formula? Explain various signal flow terms.

c) Write mathematical model of Mass, Spring and Damper element.

***Q2)*** Attempt any TWO **[2 × 8 = 16]**

a) For a unity feedback system having open loop transfer function $G(s) = k(S+13)/S(S+3)(S+7)$, Using the routh criterion, Determine the range of values of K for the system to be stable, marginal value of K and frequency of sustained oscillation.

b) Explain Reduction of parameter variations by use of feedback

c) State and derive the steady state errors and error constants for type - 0, Type - 1 and type -2 system

***P.T.O.***

*Q3)* Attempt any TWO [2 × 8 = 16]

a) Derive the time response of second order systems to unit step inputs.

b) A unity feedback control system has

G(S)=K/ S(S+2)(S+5)

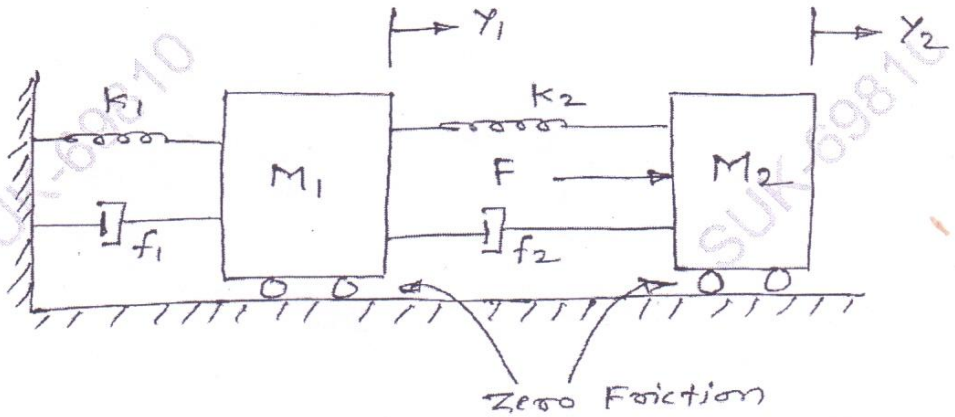
Sketch the root locus and show on it

i) Breakaway point

ii) Line for $\zeta = 0.5$ and value of K for this damping ratio.

iii) The frequency at which the root locus crosses the imaginary axis and the corresponding value of k.

c) For the mechanical system shown in fig below, obtain F-V analogous electric network.




## SECTION - II

*Q4)* Attempt any Two [16]

a) Explain frequency domain specifications .and derive expressions for any two.

b) Sketch the Bode plot for G(s)=10/s(1+ 0.5s)(1 + 0.1s) and Determine Gain Margin and Phase Margin.

c) Explain effect of addition of poles and zeros on Bode plot.

*Q5)* Attempt any Two **[16]**

a) Explain concept of state,state variable and state model

b) Check for controllability and observability

$$\begin{bmatrix} x1 \\ x2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -2 \end{bmatrix} \begin{bmatrix} x1 \\ x2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} U$$

$$y(t) = [1 \;\; 2] \begin{bmatrix} x1 \\ x2 \end{bmatrix}$$

c) Derive the equation for transfer function from state model for continuous time system

*Q6)* Attempt any Three **[18]**

a) Lead-lag compensator

b) PI Controller

c) Nyquist Stability Criterion

d) Polar plot

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